Appl. No. 10/772,064 Amdt. dated March 28, 2006 Reply to Office Action of December 28, 2005

PATENT

REMARKS/ARGUMENTS

This Amendment is responsive to the Office Action mailed on December 28, 2006. In this Amendment, claims 2-3 are amended so that they are in independent form, non-elected claims 10-20 are canceled, and claims 21-26 are added so that claims 1-9 and 21-26 are pending and subject to examination.

The amendments to claims 2-3 do not raise new issues requiring further search and/or consideration as these claims are merely put into independent form.

I. 35 USC 102(b) - Mehringer et al.

In the Office Action, claims 1, 5, 6, and 9 are rejected as anticipated by Mehringer et al. (U.S. Patent No. 5,869,883). According to the Examiner, Mehringer et al. discloses "mounting a semiconductor die to the die attach region using a flip chip mounting process, col. 9, [lines] 9-55". This rejection is traversed.

Mehringer et al. does not anticipate the present claims, since Mehringer et al. does not teach each and every element of the claims. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co: of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Here, Mehringer et al. does not teach or suggest, *inter alia*, "mounting a semiconductor die to the die attach region using a flip chip mounting process". Contrary to the Examiner's allegation, neither column 9, lines 9-55, nor any other portion of Mehringer et al. discloses a flip chip mounting process. Column 9, lines 9-55, of Mehringer et al. describes the embodiments in FIGS. 1 and 2. FIGS. 1 and 2 of Mehringer et al. do not even show a die, and therefore cannot teach or suggest a "flip chip mounting process".

It is clear that Mehringer et al. does <u>not</u> disclose a flip chip mounting process. As is well known in the art, a "flip chip mounting process" is a process whereby a chip (or die) has a conductive material such as solder deposited on one side of the chip. The chip is then "flipped" over and mounted onto a leadframe, circuit board, or the like. See FIG. 4(c) in the present

Appl. No. 10/772,064 Amdt. dated March 28, 2006 Reply to Office Action of December 28, 2005

PATENT

application. In contrast, as shown in FIGS. 6, 7, 8, 9, and 10 of Mehringer et al., Mehringer et al.'s die is never coated with a conductive material and flipped. Rather, the die is mounted on a die paddle 16 and the top is "wire-bonded" to the terminals 17. The differences between the "wire-bonding" process disclosed in Mehringer et al. and a flip chip process are shown in the attached Web pages describing the term "flip chip" at "http://computing-dictionary.thefreedictionary.com/flip+chip". Since Merhinger et al. does not disclose or suggest a "flip chip" mounting process, Merhinger et al. cannot anticipate claims 1, 5, 6, and 9, and withdrawal of the anticipation rejection is requested.

II. 35 USC 103 - Mehringer and Joshi et al.

Claims 2, 3, 4, 7, and 8 are rejected as being obvious over Mehringer et al. and Joshi et al. (U.S. Publication No. 2003/0075786). This rejection is traversed.

Joshi et al. cannot be used to render the claims obvious. 35 U.S.C. § 103(c)(1)

states:

(c) (1) Subject matter developed by another person, which qualifies as prior art only under one or more of subsections (e), (f), and (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the claimed invention was made, owned by the same person or subject to an obligation of assignment to the same person.

If it is prior art at all, Joshi et al. would be prior art under 35 U.S.C. § 102(e) and is owned by the same assignee as the present application. In this regard, the undersigned states:

Application 10/271,654, corresponding to United States Patent Application Publication 2003/0075786, and the present application U.S. Patent Application No. 10/772,064, were, at the time the invention of U.S. Patent Application No. 10/772,064 was made, owned by Fairchild Semiconductor Corp.

Appl. No. 10/772,064 Amdt. dated March 28, 2006 Reply to Office Action of December 28, 2005

PATENT

Since Joshi et al. cannot be used to render the claims obvious pursuant to MPEP § 706.02(1)(2) and 35 U.S.C. 103(c), withdrawal of the rejection is requested.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

Patrick R. Jewik Reg. No. 40,456

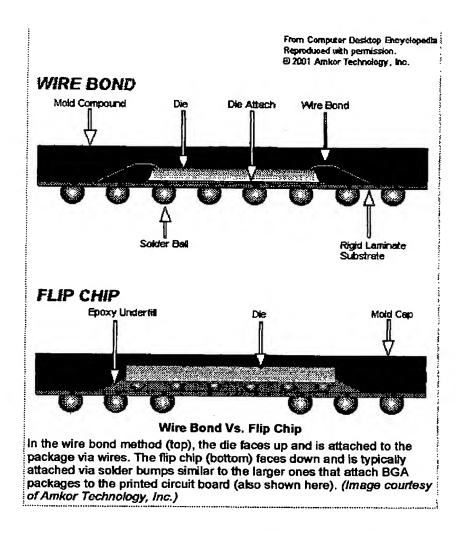
TOWNSEND and TOWNSEND and CREW LLP Two Embarcadero Center, Eighth Floor San Francisco, California 94111-3834 Tel: 415-576-0200

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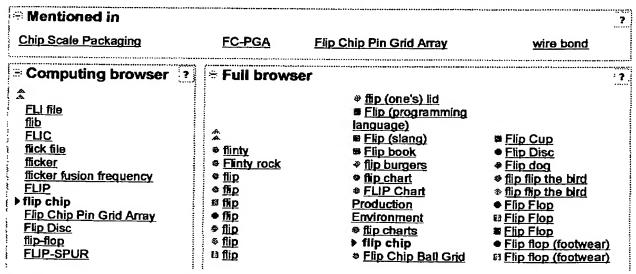
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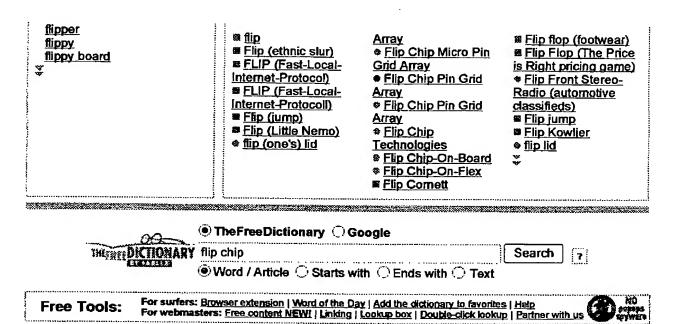


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http://computing-dictionary.thefreedictionary.com/flip+chip

3/27/2006



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